SILERGY

Application Notes: AN_SY6983

High Efficiency, 1A, Three-Cell Boost Li-Ion Battery Charger

General Description

SY6983 is a 3.6-10V_{IN}, 1A three-cell synchronous boost Li-Ion battery charger which integrates 500kHz switching frequency and full protection functions. The charge current up to 1A can be programmed by using an external resistor for different portable applications and indicating the charge current information simultaneously. It also has a programmable charge timeout for safe battery charge operation and a programmable input voltage threshold for adaptive input current limit. SY6983 can disconnect output when there is an output short circuit or shutdown. It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

SY6983 along with small QFN3×3 footprint provides small PCB area application.

Ordering Information

SY6983 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY6983QDC	QFN3×3-16	----

Features

- Low Profile QFN3×3 Package
- Integrated Synchronous Boost with 18V Rating Low R_{DSON} FETs for High Charge Efficiency
- Trickle Current / Constant Current / Constant Voltage Charge Mode
- Programmable Input Voltage Threshold for Adaptive Current Limit
- Maximum 1A Constant Charge Current
- Charge Current Information Indication
- Programmable Charge Timeout
- Programmable Constant Charge Current
- Selectable Constant Voltage
- ±0.5% Battery Voltage Accuracy
- Thermal Regulation Protection
- External Shutdown Function
- Input Voltage UVLO and OVP
- Over Temperature Protection
- Output Short Circuit Protection
- Charge Status Indication
- Normal Synchronous Boost Operation When the Battery is Removed

Applications

- Cellular Telephones, PDA, MP3 Players, MP4 Players
- Digital Cameras
- Bluetooth Applications
- PSP Game Players, NDS Game Players
- Notebook

Typical Application

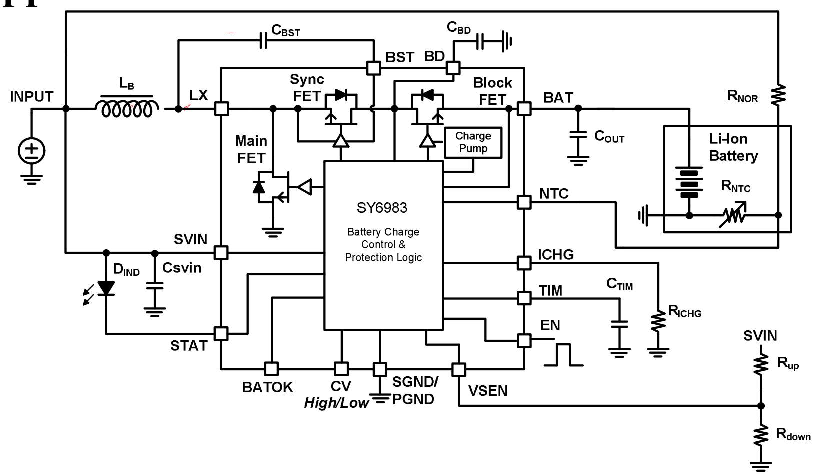
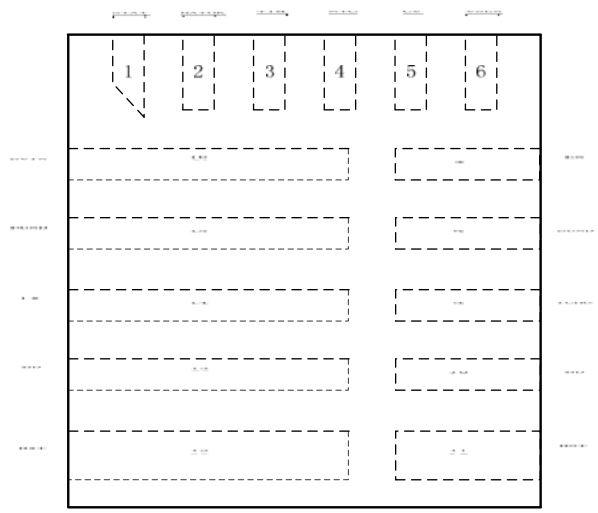


Figure1. Schematic Diagram

Pinout (Top View)



(QFN3×3-16)

Top Mark: **BQW***xyz*, (Device code: **BQW**, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
STAT	1	Charge status indication pin. It is an open drain output pin and pulling high to SVIN through a LED which indicates the charge in process. When the charge is done, LED is off.
BATOK	2	Good battery present indication pin. When V is lower than 9.1V, or NTC is pulled up to SVIN, BATOK pin will output low logic to turn off the system operation. Otherwise, BATOK pin will output high logic to turn on the system operation.
TIM	3	Charge time limit pin. Connect this pin with a capacitor to ground. Internal current source charge the capacitor for TC mode and CC mode's charge time limit. TC charge time limit is about 1/10 of CC charge time limit.
NTC	4	Thermal protection pin. UTP threshold is typically 75% of V_{SVIN} and OTP threshold is typically 46.5% of V_{SVIN}. Pulling up to SVIN can disable charge logic and make the IC operate as a normal boost regulator. If it is pulled down to the ground, the IC can be shutdown.
CV	5	Battery CV voltage selection pin. Pull down for 12.6V CV voltage and pull up for 13.05V CV voltage.
VSEN	6	Voltage sense of SVIN. If the voltage drops to internal 1.2V reference voltage, the SVIN will be clamped to set value and the input current will be limited.
EN	7	Enable control pin. High logic for enable on, and low logic for enable off.
SGND	8	Signal ground pin.
ICHG	9	Charge current program pin. Pull down to GND with a resistor $R_{ICHG.}$ The mirror current about 1/10000 of the blocking FET current will dump into the external RC network through ICHG pin and be compared to the internal reverence 1V. So I_{CC}=(1V/ R_{ICHG})x10k, I_{TC}=(1V/ R_{ICHG})x1k.
BD	10, 13	Connect to the Drain of internal Blocking FET. Bypass at least 4.7µF ceramic cap to GND.
BST	11	Boost-Strap pin. Supply Rectified FET's gate driver. Decouple this pin to LX with a 0.1µF ceramic cap.
BAT	12	Battery positive pin.
LX	14	Switch node pin. Connect it to the external inductor.
PGND	15	Power ground pin.
SVIN	16	Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage range.

Absolute Maximum Ratings

STAT, NTC, CV, VSEN, EN, ICHG, BD, BAT, LX, SVIN---------- 18V
BATOK, TIM, BST-LX ---------- 4V
LX Pin Current Continuous ---------- 5A
Power Dissipation, P_D @ T_A = 25°C, QFN3×3 ---------- 2.6W
Package Thermal Resistance
θ_{JA} ---------- 38°C/W
θ_{JC} ----------4°C/W
Junction Temperature Range ---------- -40°C to +125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 125°C

Recommended Operating Conditions

SVIN ---------- 3.6V to 10V
STAT, NTC, CV, VSEN, EN, ICHG, BD, BAT, LX, ---------- -0.3V to 16V
BATOK, TIM ---------- -0.3V to 3.3V
LX Pin Current Continuous ---------- 5A
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

T_A=25°C, V_{IN}=5V, GND=0V, C_{IN}=22μF, L=2.2μH, R_{ICHG}=10kΩ, C_{TIM}=470nF, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Bias Supply (V_{SVIN})						
V_{SVIN}	Supply Voltage		3.6		10	V
V_{UVLO}	V_{SVIN} Under Voltage Lockout Threshold	V_{SVIN} rising and measured from V_{SVIN} to GND			3.5	V
ΔV_{UVLO}	V_{SVIN} Under Voltage Lockout Hysteresis	Measured from V_{SVIN} to GND		100		mV
V_{OVP}	Input Overvoltage Protection	V_{SVIN} rising and measured from V_{SVIN} to GND	10			V
ΔV_{OVP}	Input Overvoltage Protection Hysteresis	Measured from V_{SVIN} to GND		0.5		V
Quiescent Current						
I_{BAT}	Battery Discharge Current	Shutdown IC, EN=NTC=0			25	μA
I_{IN}	Input Quiescent Current	Disable Charge, EN=1,NTC=0			1.5	mA
Oscillator and PWM						
f_{SW}	Switching Frequency			500		kHz
T_{MINOFF}	Main N-FET Minimum OFF Time	With 18V rating		100		ns
T_{MAXOFF}	Main N-FET Maximum OFF Time	With 18V rating		30		μs
T_{MINON}	Main N-FET Minimum ON Time	With 18V rating		100		ns
Power MOSFET						
R_{NFET_M}	$R_{DS(ON)}$ of Main N-FET			80		mΩ
R_{NFET_R}	$R_{DS(ON)}$ of Rectified N-FET			40		mΩ
R_{NFET_B}	$R_{DS(ON)}$ of Blocking N-FET			40		mΩ
Voltage Regulation						
V_{CV}	3-Cell CV Charge Mode Voltage	<1V	12.537	12.6	12.663	V
		V_{CV}>2V	12.985	13.05	13.115	
V_{CVH}	High Level Logic for CV		2			V
V_{CVL}	Low Level Logic for CV				1	V
ΔV_{RCH}	3-Cell Recharge Voltage		150	300	450	mV
V_{TRK}	3-cell TC Charge Mode Battery Voltage Threshold	V_{SVIN} ≤8V rising edge threshold	8.1	8.4	8.7	V
		V_{SVIN}>8V rising edge threshold		1.066		V_{SVIN}
Battery Connect Detection						
V_{DET}	NTC Voltage Threshold for Battery Detect	NTC falling edge	85%		95%	V_{SVIN}
t_{DET}	Detect Delay Time			30		ms
Charge Current						
	Internal Charge Current Accuracy for Constant Current Mode	I_{CC}=1000mA	-10%		10%	
	Internal Charge Current Accuracy for Trickle Current Mode	I_{TC}=100mA	-50%		50%	
I_{TERM}	Termination Current	I_{CC}=1000mA	50	100	150	mA
Output Voltage OVP						
V_{OVP}	Output Voltage OVP Threshold		105%	110%	115%	V_{CV}
Input Voltage Threshold for Adaptive Current Limit						

$V_{Threshold}$	Voltage Reference of VSEN	$V_{SVIN} \le 6V$	1.171	1.195	1.219	V
ΔV_{AICL}	The Adaptive Input Power Limit Reference is $V_{SVIN}-\Delta V_{AICL}$	$V_{SVIN} > 6V$		0.6		V
Timer						
T_{TC}	Trickle Current Charge Timeout	C_{TIM}=330nF	0.23	0.5	0.67	hour
T_{CC}	Constant Current Charge Timeout		3.0	4.5	6	hour
T_{MC}	Charge Mode Change Delay Time			30		ms
T_{TERM}	Termination Delay Time			30		ms
T_{RCHG}	Recharge Time Delay			30		ms
Short Circuit Protection						
ΔV_{SHORT}	Output Short Protection Threshold is $V_{SVIN}-\Delta V_{SHORT}$			2		V
BATOK Indication						
V_{BATOKH}	BATOK High Voltage Output			3		V
V_{BATOKL}	BATOK Low Voltage Output			0		V
Linear Charger Mode						
I_{LCHG}	Battery Charger Current When the Blocking FET is in Linear Mode	$V_{BAT}<V_{SHORT}$		10%		I_{CC}
I_{LPEAK}	Peak Linear Current When Battery is Absent			1		A
V_{BD}	Bus Voltage Regulation	$V_{SVIN} \le 8V$		9.24		V
		$V_{SVIN}>8V$		1.156		V_{SVIN}
V_{TRON}	Blocking FET Fully Turn On Threshold $V_{TRON}=V_{BAT}-S_{VIN}$	$V_{BAT} > V_{TRK}$		100		mV
Enable ON/OFF Control						
V_{ENH}	High Level Logic for Enable Control		1.5			V
V_{ENL}	Low Level Logic for Enable Control				0.4	V
Battery Thermal Protection NTC						
UTP	Under Temperature Protection		70%	75%	80%	V_{SVIN}
	Under Temperature Protection Hysteresis	Falling edge		5%		
OTP	Over Temperature Protection		45%	46.5%	48%	
	Over Temperature Protection Hysteresis	Rising edge		2%		
Thermal Regulation and Thermal shutdown						
T_{REG}	Thermal Regulation Threshold	Rising threshold		120		ºC
T_{REGHYS}	Thermal Regulation Hysteresis Falling Edge			20		ºC
	Thermal Regulation Fold Back Ratio			0.25		I_{CC}
T_{SD}	Thermal Shutdown Temperature	Rising threshold		160		ºC
T_{SDHYS}	Thermal Shutdown Temperature Hysteresis			20		ºC

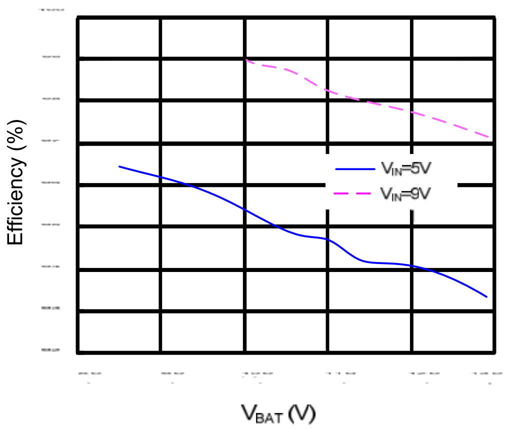
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A = 25°C$ on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

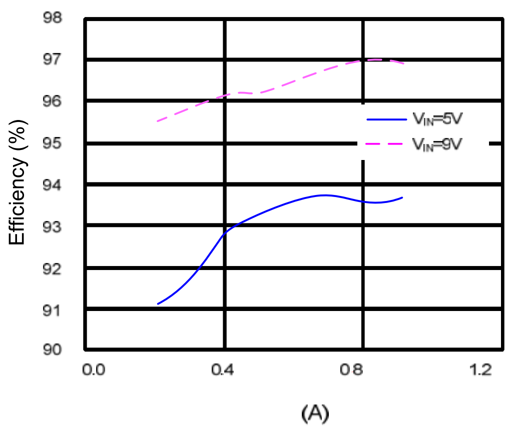
Note 3: The device is not guaranteed to function outside its operating conditions

Typical Performance Characteristics

Efficiency VS BAT Voltage (CC mode)

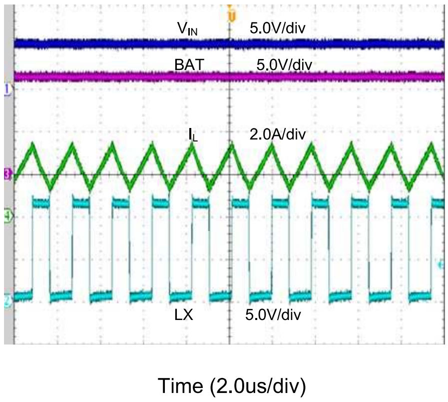


Efficiency VS Charge Current(CV mode)



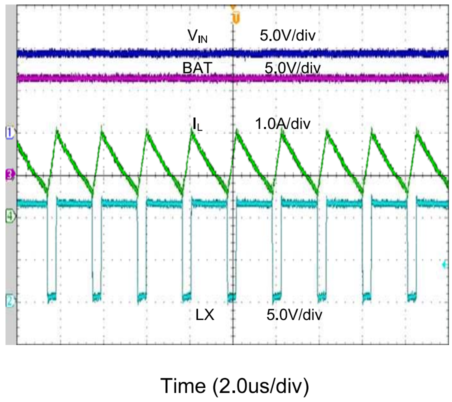
Steady Waveforms (CC Mode)

(V_{IN}=5.0V, V_{BAT}=11V)



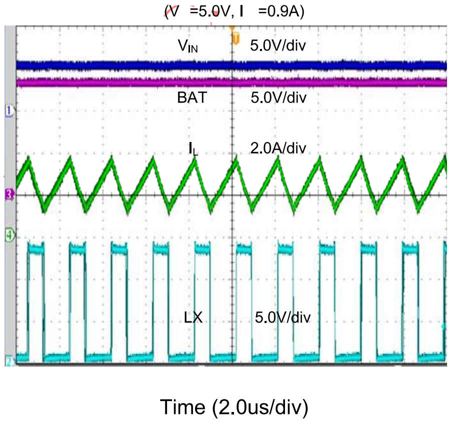
Steady Waveforms (CC Mode)

(V_{IN}=9.0V, V_{BAT}=11V)



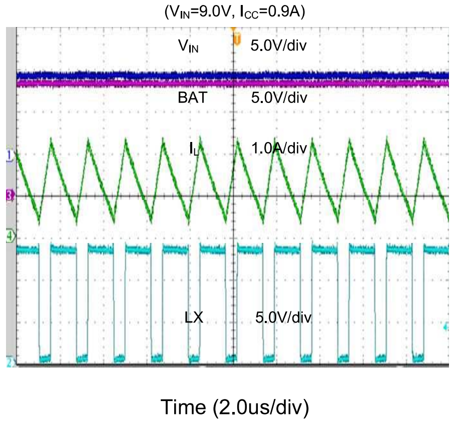
Steady Waveforms (CV Mode)

(V =5.0V, I =0.9A)



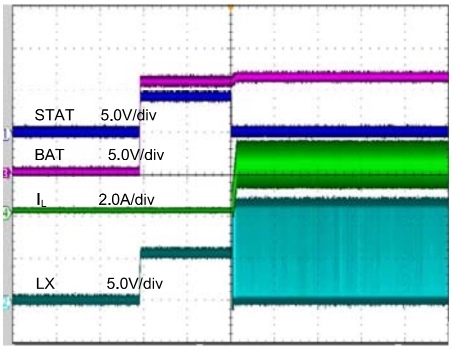
Steady Waveforms (CV Mode)

(V_{IN}=9.0V, I_{CC}=0.9A)



Power ON (CC Mode)

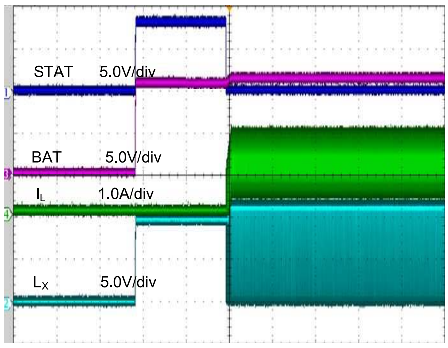
(V_{IN}=5.0V, V_{BAT}=11V)



Time (400ms/div)

Power ON (CC Mode)

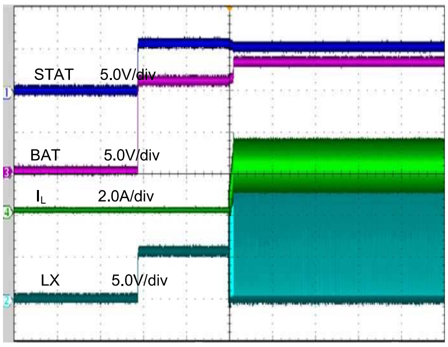
(V_{IN}=9.0V, V_{BAT}=11V)



Time (400ms/div)

Power ON (CV Mode)

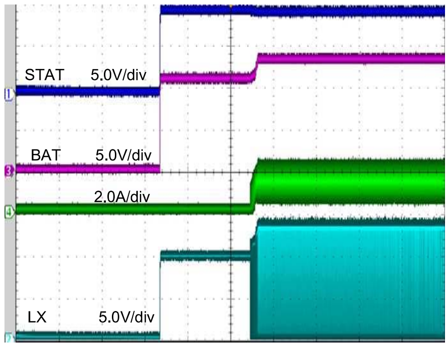
(V_{IN}=5.0V, I_{CC}=0.9A)



Time (400ms/div)

Power ON (CV Mode)

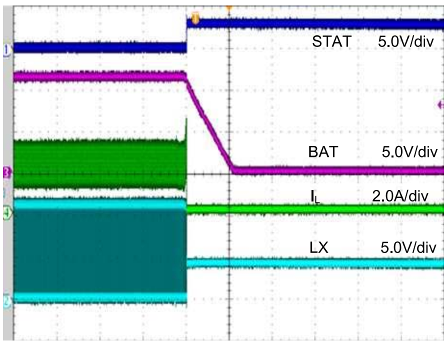
(V_{IN}=9.0V, I_{CC}=0.9A)



Time (400ms/div)

Power OFF (CC Mode)

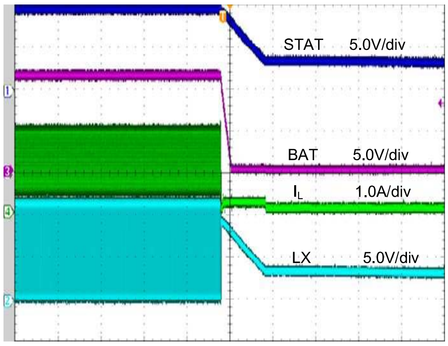
(V_{IN}=5.0V, V_{BAT}=11V)



Time (2ms/div)

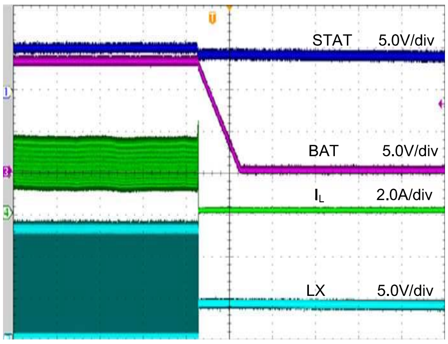
Power OFF (CC Mode)

(V_{IN}=9.0V, V_{BAT}=11V)



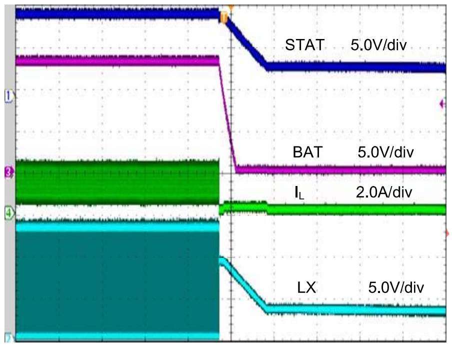
Time (10ms/div)

Power OFF (CV Mode)
(V_{IN}=5.0V, I_{CC}=0.9A)



Time (4ms/div)

Power OFF (CV Mode)
(V_{IN}=9.0V, V_{BAT}=11V)



Time (10ms/div)

General Function Description

SY6983 is a 3.6-10V_{IN}, 1A three-cell synchronous boost Li-Ion battery charger which integrates 500kHz switching frequency and full protection functions. The charge current up to 1A can be programmed by using an external resistor for different portable applications and indicating the charge current information simultaneously. It also has a programmable charge timeout for safe battery charge operation and a programmable input voltage threshold for adaptive input current limit. SY6983 can disconnect output when there is an output short circuit or shutdown. It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

Charging Status Indication Description

1. Charge-In-Process – Pull and keep STAT pin to Low;
2. Charge Done – Pull and keep STAT pin to High;
3. Fault Mode –High output and low voltage alternately at the frequency of 1.3Hz. Connecting a LED from SVIN to STAT pin, LED ON means Charge-in-Process, LED OFF means Charge Done, LED Flashing with 1.3Hz means Fault Mode.

Switching Mode Boost Charger Basic Operation Description

Switching Mode Control Strategy

SY6983 is a switching mode Boost charger for the applications with USB power input. The 500kHz fixed frequency is easy for the size minimization of peripheral circuit design.

Operation Principle

SY6983 can normally work with or without Li-Ion battery.

Battery Present

When the battery is present, SY6983 will work on trickle current charging, constant current charging and constant voltage charging mode according to different battery voltage.

Battery Absent

If there's no battery connection detected through NTC pin, SY6983 will operate as a normal switching mode boost converter. The internal constant current loop and voltage loop are both active.

Basic Protection Principle

SY6983 has sufficient battery charging protection. When the input over voltage protection, the output over voltage protection, the thermal protection or the timeout protection happens, the boost charger will stop switching immediately. When the V is lower than V_{SHORT}, the short circuit protection will happen. The main FET will be turned off firstly. The block FET will enter linear mode with 1/10 I_{CC} charging current. When V_{BAT} goes back to be higher than V_{SHORT}, the boost charger will restart to work at light load and regulate V_{BD} at Max[9.24V,1.15×V_{SVIN}], linear charge current will be 1/10 I_{CC}. When V_{BAT} goes back to be higher than V_{TRK}, the boost switching charger will take it over.

Adaptive Input Current Limit Principle

SY6983 can limit the input power adaptively and adjust this threshold according to the input voltage. It will automatically decrease charge current when V_{SVIN} voltage drops to adaptive input power limit reference Vref.

For typical 5V adapter, Vref is set by VSEN pin, that is calculated as：

$$Vref = 1.2 \times \frac{R_{UP} + R_{DN}}{R_{DN}}$$

If V_{SVIN} voltage is higher than 6V, Vref is calculated as:

$$Vref = V_{SVIN} - \Delta V_{AICL}$$

Where ΔV_{AICL} is 0.6V, V_{SVIN} is the input voltage when adapter inserts.

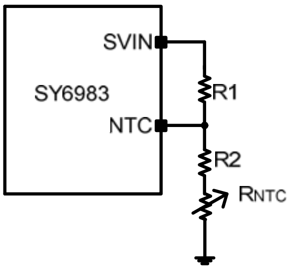
Constant Voltage Threshold Program Principle

SY6983 can program the constant voltage threshold through the CV pin. When V_{CV} is higher than 2V, the constant voltage threshold will be 13.05V; when V_{CV} is lower than 1V, the constant voltage threshold will be 12.6V.

Applications Information

Because of the high integration of SY6983, the application circuit is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L, NTC resistors R1, R2, input voltage threshold resistors R_{up}, R_{down} and timer capacitor C_{TIM} need to be selected for the target applications specifications.

NTC resistor:
SY6983 monitors battery temperature by measuring the input voltage and NTC voltage. The controller will trigger the UTP or OTP when the rate K (K= VNTC/VSVIN) reaches the threshold of UTP (KUT) or OTP (KOT). The temperature sensing network is showed as below.
Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps are:

1. Define K_{UT}, K_{UT} =70~80%
2. Define K_{OT}, K_{OT} =45~48%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R2,
$$R2=\frac{K_{OT}(1-K_{UT})R_{UT}-K_{UT}(1-K_{OT})R_{OT}}{K_{UT}-K_{OT}}$$
5. Calculate R1
$$R1=(1/K_{OT}-1)(R2+R_{OT})$$

If choose the typical values KUT =75% and KOT=46.5%, then
$$R2=0.408R_{UT}-1.408R_{OT}$$
$$R1=1.151(R2+R_{OT})$$

Timer capacitor C_{TIM}
The charger also provides a programmable charge timer. The charge time is programmed by the capacitor connected between the TIM pin and GND pin. The capacitance is given by the formula:
$$C_{TIM}=2\times10^{-11}T_{CC}\quad\text{, unit: f.}$$
T_{CC} is the target constant charge time, unit: s.

Input capacitor C_{IN}:
The ripple current through input capacitor is greater than
$$I_{CIN\_RMS}=\frac{V_{IN}\times(V_{OUT}-V_{IN})}{2\sqrt{3}\times L\times F_{SW}\times V_{OUT}}$$
X5R or X7R ceramic capacitors with greater than 4.7µF capacitance are recommended to handle this ripple current.

Output capacitor C_{OUT}:
The output capacitor is selected to handle the output ripple requirement. This ripple voltage is related to the capacitance and its equivalent series resistance (ESR). For the best performance, it is recommended to use X5R or better grade low ESR ceramic capacitor. The voltage rating of the output capacitor should be higher than the maximum output voltage. The minimum required capacitance can be calculated as:
$$C_{OUT}=\frac{I_{CC}\times(V_{OUT}-V_{IN})}{F_{SW}\times V_{OUT}\times V_{RIPPLE}}$$
Where V_{RIPPLE} is the peak to peak output ripple and I_{CC} is the set charge current.
For SY6983, the output capacitor is paralleled by C_{BD} for less output ripple and each capacitor with greater than 10µF capacitance is recommended.

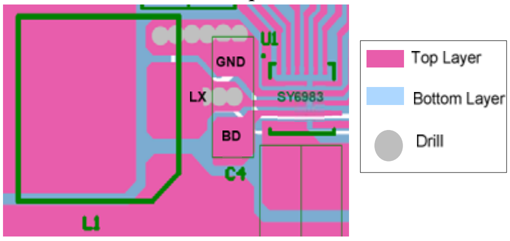
Inductor L:
There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:
$$L=\left(\frac{V_{IN}}{V_{OUT}}\right)^2\frac{(V_{OUT}-V_{IN})}{I_{CC}\times F_{SW}\times 40\%}$$
Where F_{SW} is the switching frequency and I_{CC} is the set charge current.
The SY6983 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.
$$I_{SAT,MIN}>\left(\frac{V_{OUT}}{V_{IN}}\right)\times I_{CC}+\left(\frac{V_{IN}}{V_{OUT}}\right)^2\frac{(V_{OUT}-V_{IN})}{2\times F_{SW}\times L}$$
3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve good overall efficiency.

Layout Design:

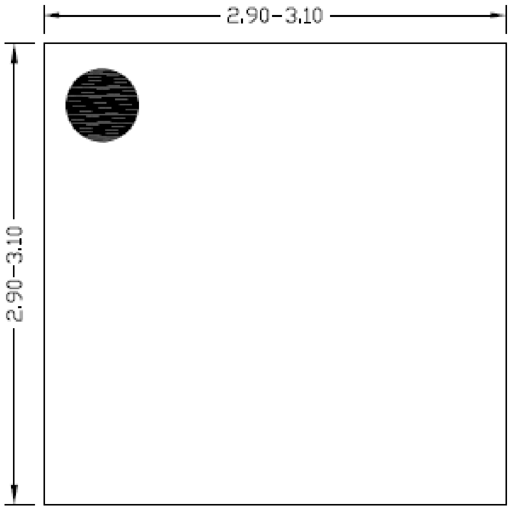
The layout design of SY6983 regulator is relatively simple. For the best efficiency and to minimize noise problems, we should place the following components close to the IC: C_{SVIN}, L, C_{BD}.

1) The loop of main MOSFET, rectifier diode, and C_{BD} must be as short as possible

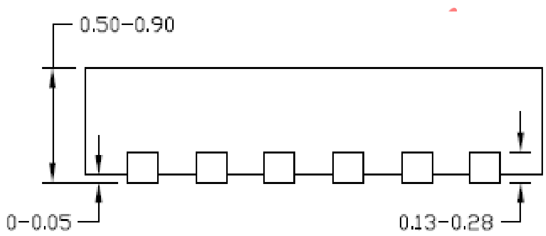


2) It is desirable to maximize the PCB copper area adjacent to GND pin to achieve the best thermal performance and noise performance.
3) C_{SVIN} must be close to pin SVIN and GND.
4) The PCB copper area adjacent to LX pin must be minimized to avoid the potential noise problem.
5) The small signal components R_{ICHG} , R_{up} and R_{down} must be placed close to the IC but not be adjacent to the LX net on the PCB layout to avoid noise problem.

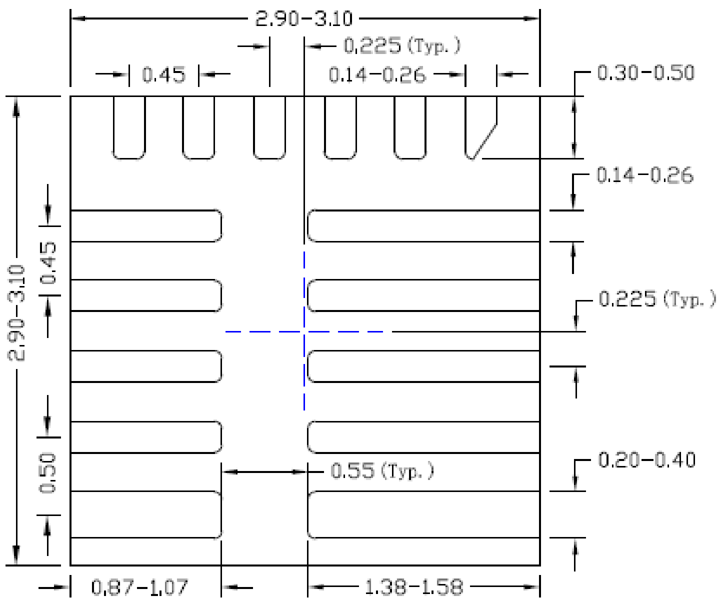
QFN3×3-16 FC Package Outline Drawing



Top View



Side View



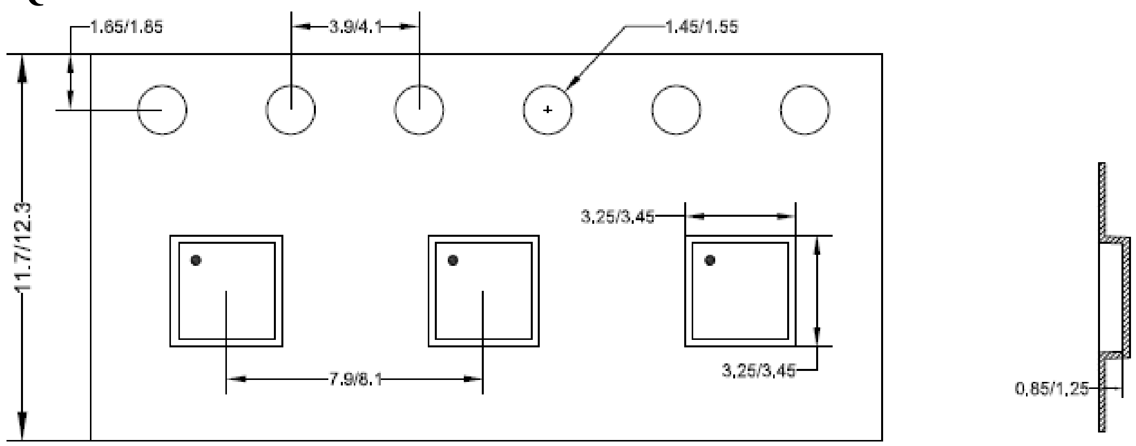
Bottom View

Notes: All dimension in millimeter and exclude mold flash & metal burr.

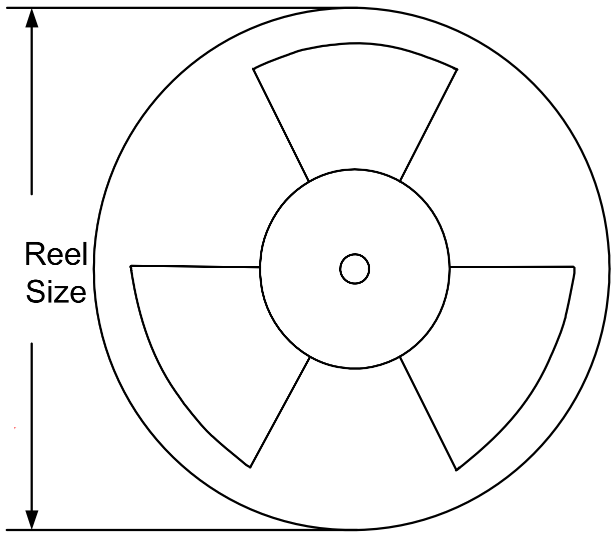
Taping & Reel Specification

1. Taping orientation

QFN3×3



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA