Applications Note:AN_SY8101A/B/C/D

High Efficiency 400KHz, 0.6A/1A/1.5A/2A, 16V Input Synchronous Step Down Regulator

Preliminary SPECIFICATION

General Description

The SY8101A, SY8101B, SY8101C and SY8101D are high efficiency 400KHz synchronous step-down DC-DC converters capable of delivering 0.6A, 1A, 1.5A, 2A output currents, respectively. SY8101A/B/C/D operate over a wide input voltage range from 4V to 15V and integrate main switch and synchronous switch with very low Rds(on) to minimize the conduction loss.

Low output voltage ripple and small external inductor and capacitor sizes are achieved with 400KHz switching frequency.

Features

- low Rds(on) for internal switches (top/bottom)
  - SY8101A: 300/200 mΩ, 0.6A
  - SY8101B: 200/150 mΩ, 1A
  - SY8101C: 150/120 mΩ, 1.5A
  - SY8101D: 120/90 mΩ, 2A
- 4-15V input voltage range
- 400kHz switching frequency
- Internal softstart limits the inrush current
- 2% 0.6V reference
- RoHS Compliant and Halogen Free
- Compact package: SSOT23 6 pin

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Ordering Information

SY8101□(□□)□

- Temperature Code: C: 0°C~85°C
- Package Code: EB: SSOT23-6
- Spec Code

Typical Applications

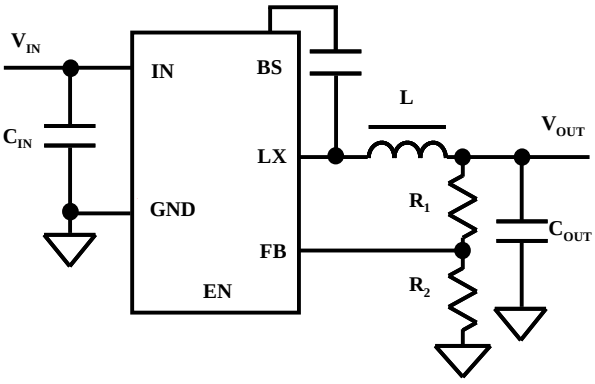


Figure 1. Schematic Diagram

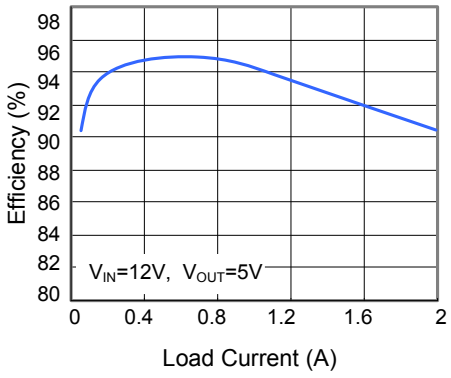
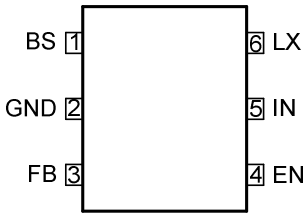


Figure 2. Efficiency vs Load Current

Pinout (top view)



(SSOT23-6)

Top Mark: **CF*xyz*** for SY8101A, **BJ*xyz*** for SY8101B, **BM*xyz*** for SY8101C, **CG*xyz*** for SY8101D
(Device code: CF for SY8101A, etc.; ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1uF ceramic cap.
IN	5	Input pin. Decouple this pin to GND pin with at least 1uF ceramic cap
LX	6	Inductor pin. Connect this pin to the switching node of inductor
GND	2	Ground pin
FB	3	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=0.6*(1+R1/R2)
EN	4	Enable control. Pull high to turn on. Do not float.

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 16V
Enable, FB Voltage---------- V_{IN} + 0.6V
Power Dissipation, P_D @ T_A = 25°C SSOT23-6, ---------- 0.4W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 250°C/W
θ_{JC} ---------- 130°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
ESD Susceptibility (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 15V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 2.5V, L = 2.2uH, C_{OUT} = 10uF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		15	V
Quiescent Current	I_Q	$I_{OUT=0}$, VFB=VREF+5%		200		μA
Shutdown Current	I_{SHDN}	EN=0		1	5	μA
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
FB Input Current	I_{FB}	VFB=VIN	-50		50	nA
Top FET RON	Rds(on)1	SY8101A		0.3		Ω
		SY8101B		0.2		Ω
		SY8101C		0.15		Ω
		SY8101D		0.12		Ω
Bottom FET RON	Rds(on)2	SY8101A		0.2		Ω
		SY8101B		0.15		Ω
		SY8101C		0.12		Ω
		SY8101D		0.09		Ω
Top FET Current Limit	I_{LIM}	SY8101A	0.9			A
		SY8101B	1.3			A
		SY8101C	1.8			A
		SY8101D	2.4			A
EN rising threshold	V_{ENH}		1.5			V
EN falling threshold	V_{ENL}				0.4	V
Input UVLO threshold	V_{UVLO}				3.9	V
UVLO hysteresis	V_{HYS}			0.3		V
Oscillator Frequency	F_{OSC}	IOUT=200mA		0.4		MHz
Min ON Time				50		ns
Max Duty Cycle			90			%
Thermal Shutdown Temperature	T_{SD}			160		°C

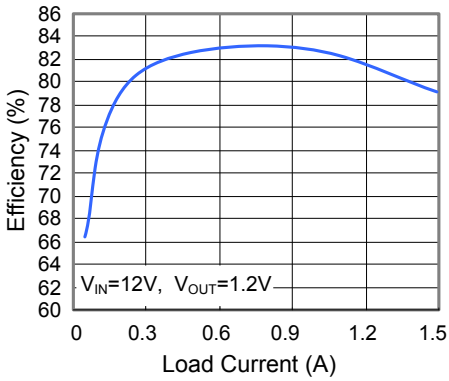
Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θJA is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Pin 2 of SSOT-23-6 packages is the case position for JC measurement.

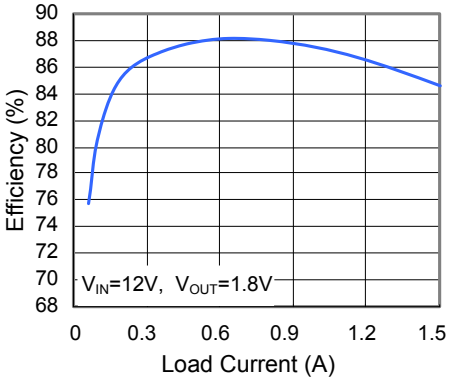
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics（SY8101C）

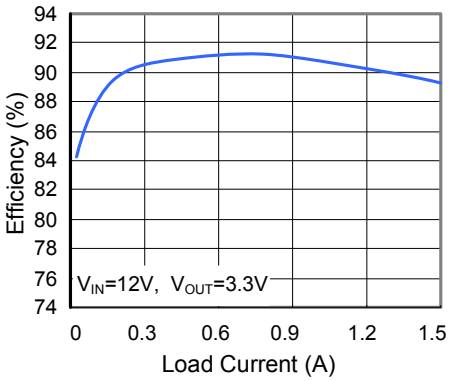
Efficiency vs Load Current



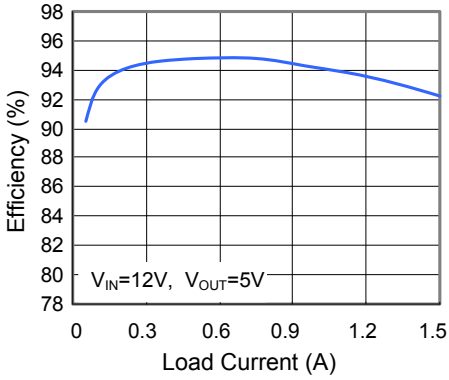
Efficiency vs Load Current



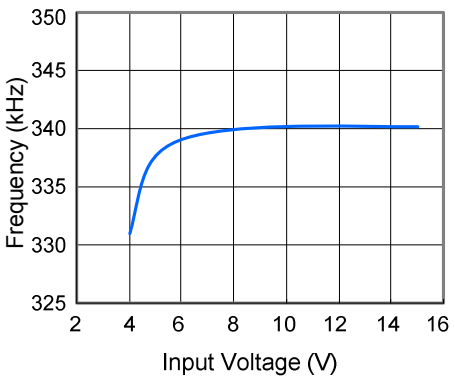
Efficiency vs Load Current



Efficiency vs Load Current

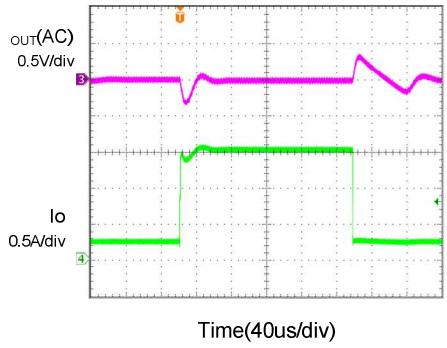


Oscillator Frequency vs V_{IN}



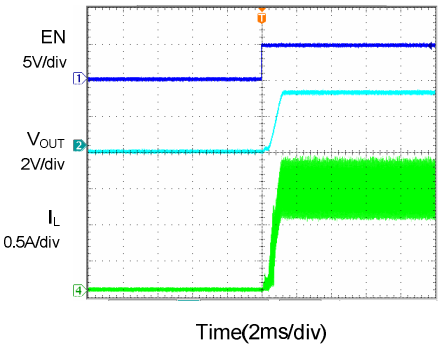
Load Transient

(V_{IN}=12V, V_{OUT}=3.3V,Iload=0.15~1.5A)



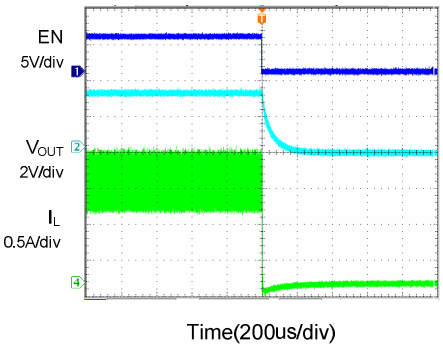
Startup

(V_{IN}=12V, V_{OUT}=3.3V,Iload=1.5A)



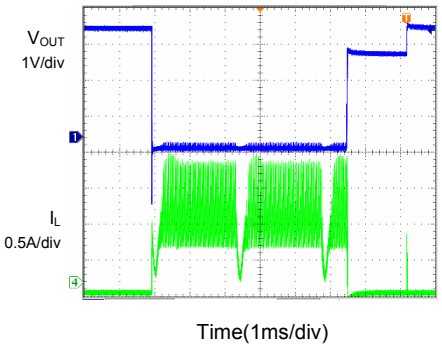
Shutdown

(V_{IN}=12V, V_{OUT}=3.3V,Iload=1.5A)



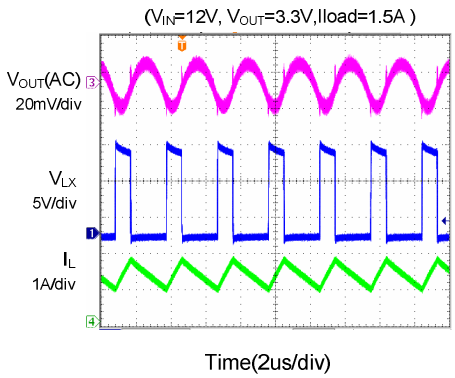
Short Circuit Protection

(V_{IN}=12V, V_{OUT}=3.3V,Open to short)



Output Ripple

(V_{IN}=12V, V_{OUT}=3.3V,Iload=1.5A)



Operation

SY8101 is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low Rds(on) power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

Applications Information

Because of the high integration in the SY8101 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R1 and R2:

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 100k and 1M is highly recommended for both resistors. If R2=120k is chosen, then R1 can be calculated to be:

$$R1 = \frac{(V_{OUT} - 0.6\,V)\cdot(R2)}{0.6V}$$

Input capacitor C_{IN}:

With the maximum load current at 2A, the maximum ripple current through input capacitor is about 0.6Arms. A typical X7R or better grade ceramic capacitor with 6V rating and greater than 4.7uF capacitance can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor with 6V rating and greater than 4.7uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and I_{OUT}, max is the maximum load current.

The SY8101 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

Layout Design:

The layout design of SY8101 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) CIN must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

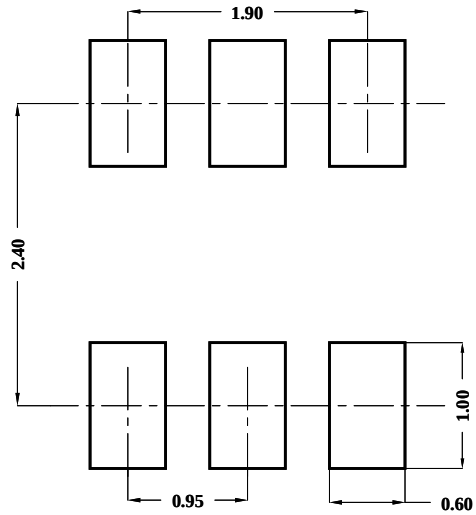
3) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

4) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

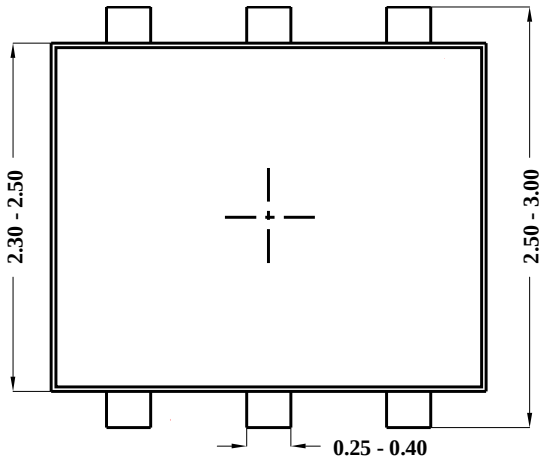
Load Transient Considerations:

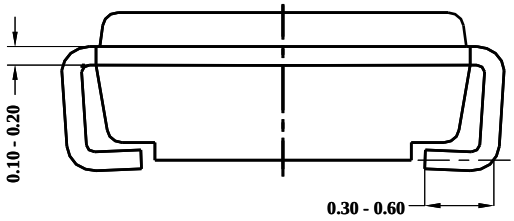
The SY8101 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

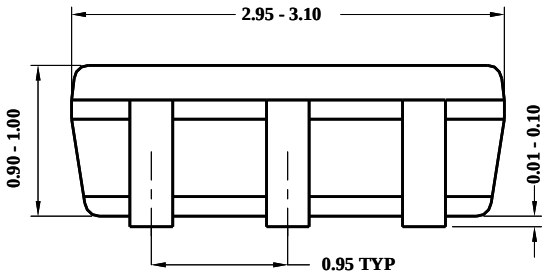
SSOT23-6 Package outline & PCB layout design



Recommended Pad Layout







Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.